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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent No.:	6909663 B1
Issued:	June 21, 2005
First Named Inventor:	Hemanshu Vernenker
Title	MULTIPORT MEMORY WITH TWISTED BITLINES

REQUEST FOR EXPEDITED ISSUANCE OF CERTIFICATE OF CORRECTION PURSUANT TO 37 CFR 1.322

Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Review of the above-identified patent has revealed errors in the patent attributable solely to the Patent and Trademark Office. Applicant therefore requests that a Certificate Of Correction be issued to correct these errors.

The location of the errors in the patent and the corresponding correct language in the application file are set forth below:

Error in Patent	Correct Language in Application File
Col. 6, line 63	Application page 12, line 10 (claim 1)
Col. 8, line 2	Application page 13, line 24 (claim 8)
Col. 8, line 30	Notice of Allowability, page 3, paragraph 8

Documentation supporting this request and a form PTO/SB/44 showing the corrections are enclosed.

08/11/05

Although no fees are believed due, the Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 501958.

Respectfully submitted,

Date: 8/11/05

By: _____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,909,663 B1

APPLICATION NO.: 10/671,756

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INVENTOR(S) : Hemanshu Vernenker et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 6, line 63: "fist" should be --first--.
Col. 8, line 2: "fist" should be --first--.
Col. 8, line 30: "first memory port at least a first row" should be --first memory port at at least a first row--.

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address of a memory cell can be written as (RA1, RA0), wherein RA1 is a most significant bit and RA0 is a least significant bit of the row address. As shown in FIG. 1A, bitlines are exchanged between the first and second rows (the rows **104, 105**) and exchanged again between the third and fourth rows (the rows **106,107**). Therefore, logical values applied to the bitlines **116, 117** for the rows **104, 107** are inverted with respect to the logical values for the rows **105, 106**. The memory driver **200** is configured so that logical values for bitcells in the middle rows **105, 106** are inverted with respect to the logical values for bitcells in the beginning and ending rows **104, 107**. A logical function RA1 XOR RA0 can be used to determine an appropriate control signal for the mux **202**. Values of RA1 XOR RA0 are listed in Table 1.

TABLE 1

Values of the logical function A1 XOR A0.

Row No.	RA1	RA0	RA1 XOR RA0
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

Application of the control signal RA1 XOR RA0 for the first and last rows (RA1 XOR RA0=0) causes the logical value applied to the mux input **210**(A) to appear at the mux output **216**. For the middle two rows, RA1 XOR RA0=1, and an inverted logical value (~A) applied to the input **212** appears at the output **216**. A similar configuration can be used for both the A- and ~A-bitlines, and the control signal for driving either the A-bitline or the ~A-bitline can be based on the RA1 XOR RA0 function.

B-memory port bitlines are also exchanged, and a bitline driver similar to the bitline driver **200** can be used to drive B-port bitlines. Because B- and ~B-bitlines are exchanged between the rows **105, 106**, a most significant bit RB1 of a row address can be used as a control input to the mux **202**, and the XOR gate **206** can be omitted.

Larger memory arrays can include bitline exchanges and bitline drivers can be configured in association with the exchanges. For a representative 3-bit, 8-row memory (a 3:8 memory), an XOR gate can be used to provide drive values to A-port bitlines. A row location can be expressed as (RA2, RA1, RA0), wherein RA2 is a most significant bit of the row address and RA0 is a least significant bit of the row address. Table 2 contains the values of the function RA2 XOR AR1.

TABLE 2

Address logic for memory port A of a 3:8 memory array.

Row	RA2	RA1	RA0	RA2 XOR RA1
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	0

Addressing of the A-port bitlines of the middle rows (rows **2, 3, 4, 5**) is inverted with respect to the rows **0–1** and rows **6–7**, and the function RA2 XOR RA1 can be used as to control the mux **202**. The B-memory port bitlines are exchanged between rows **3** and **4**, and a most significant row address bit RB2 can be used to control the mux **202**, and the XOR gate **206** can be omitted.

A representative 3-port memory **300** is illustrated in FIG. **3A** and includes rows **302–305** and columns **308–309** of memory cells **310**. A- and ~A-bitlines **320, 321** and **322, 323** for the columns **308, 309**, respectively include bitline exchanges **326–329**. B- and ~B-bitlines **330–333** include bitline exchanges **336, 337**, and C- and ~C-bitlines **340–343** include bitline exchanges **344–347**. Conductors **350, 352** are configured to be at a potential Vdd and a conductor **354** is configured to be charged to a potential Vss.

A representative column of a 3-port memory such as the memory **300** using 10-transistor bitcells shown in FIG. **3B** is illustrated in FIG. **3C**. A- and ~A-bitlines **360, 361**, B and ~B-bitlines **362, 363**, and C-and ~C-bitlines **364, 365** are configured to drive bitcells **370, 372, 374, 376**. A- and ~A-bitlines **360, 361** and C- and ~C-bitlines **363, 364** exchange in bitline regions **380, 384**, and B- and ~B-bitlines exchange in an exchange region **382**. In the example of FIG. **3B**, bitline exchanges are associated with crossovers of two bitlines, so that all bitline exchanges can be provided in two conductor layers. Bitlines can also be arranged in different orders. For example, A- and ~A-complement bitlines can be adjacent as in the example of FIG. **1A**.

Representative examples of multi-port memories that include bitline exchanges and memory array drivers configured to read and write memory cells in such memories have been described. In other examples, **2,3, 4** or more port memories can be associated with bitline exchanges associated with some or all memory ports. Bitline exchanges for such memories can be defined in two or more conductor layers, and bitline exchanges can be located at or near bitcells or located between rows or columns of bitcells. In the illustrated examples, all memory cells used in a memory are of the same configuration, but in other examples, different memory cell configurations can be used in one or more memory locations, or different memory cell configurations can be used in one or more rows and/or columns.

Bitcell arrays can also be based on a common memory cell column. For example, a memory can be based on one or more columns of bitcells such as the column shown in FIG. **3B**. In some examples, memory cell columns include memory cells of a common design. In some examples, memory cell columns are situated between one or more conductors that are at a fixed voltage. Bitline drivers for bitlines of several or all columns can be of a common design, or different bitcell drivers can be used. Memory arrays can also be based on bitcell rows.

It will be apparent that these examples can be modified in arrangement and detail, and we claim all that is encompassed by the appended claims;

We claim:

1. A memory array, comprising:

at least a first column of memory cells and a second column of memory cells, wherein the memory cells of the first column and the second column have a common logic and are associated with at least a first memory port and a second memory port;

first column bitlines in communication with the memory cells of the first column, the first column bitlines including bitlines in communication with the first memory port and the second memory port, wherein the bitlines associated with the fist memory port include a bitline exchange associated with a first selected row of memory cells and the bitlines associated with the second memory port include a bitline exchange associated with a second selected row of memory cells,

wherein the first selected row and the second selected row are different; and

second column bitlines in communication with the memory cells of the second column, the second column bitlines including bitlines in communication with the first memory port and the second memory port, wherein the bitlines associated with the first memory port include a bitline exchange associated with the first selected row of memory cells and the bitlines associated with the second memory port include a bitline exchange associated with the second selected row of memory cells.

2. The memory array of claim 1, further comprising a conductor situated between the first column of memory cells and the second column of memory cells and configured to be charged to a predetermined voltage.

3. The memory array of claim 1, wherein the conductor is configured to supply electrical power to the memory cells of at least one of the first column and the second column of memory cells.

4. The memory array of claim 1, wherein the memory cells of the first column and the second column have a common design.

5. The memory array of claim 1, wherein the memory cells are associated with a third memory port, and bitlines associated with the third memory port include bitline exchanges at one of the first selected row or the second selected row.

6. A memory, comprising:

an array of multi-port memory cells, the array associated with a plurality of columns of memory cells;

a plurality of bitlines in communication with the columns of memory cells, wherein the plurality of bitlines for each column of memory cells includes bitlines associated with the memory ports of the multi-port memory cells, wherein the bitlines associated with at least a first memory port include a bitline exchange associated with a first selected row of memory cells and the bitlines associated with at least a second memory port include a bitline exchange associated with a second selected row of memory cells, wherein the first selected row and the second selected row are different.

7. The memory of claim 6, further comprising a set of intercolumn conductors configured to be charged to at least one fixed voltage.

8. The memory of claim 7, wherein the set of intercolumn conductors includes conductors associated with a fist voltage and a second voltage.

9. The memory of claim 7, wherein the bitlines and bitline exchanges associated with a selected memory port are defined in two conductor layers.

10. The memory of claim 6, wherein each of the columns of memory cells is of a common design.

11. The memory of claim 6, wherein each of the memory cells is of a common design.

12. A method of designing a multi-port memory array, comprising:

defining a column of memory cells having bitlines associated with each of the memory ports;

associating bitline exchanges with the bitlines of at least two memory ports, wherein the bitline exchanges for the at least two memory ports are associated with different rows; and

arranging plurality of the columns of memory cells to form an array of memory cells, thereby forming a multi-port memory array.

13. A computer readable medium comprising computer executable instructions for performing the method of claim 12.

14. The method of claim 12, further comprising defining the bitlines and bitline exchanges in two conductor layers.

15. A method of reducing electrical interference in a multi-port memory, comprising:

interchanging complementary bitlines associated with a first memory port at least a first row in substantially all columns of the memory; and

interchanging complementary bitlines associated with a second memory port at at least a second row in substantially all columns of the memory, wherein the second row is different than the first row.

16. The method of claim 15, wherein the complementary bitlines associated with the first memory port are interchanged at a first set of rows and the complementary bitlines associated with the second memory port are interchanged at a second set of rows, wherein the first set of rows and the second set of rows are different.

17. The method of claim 16, wherein the first set of rows includes even-numbered rows and the second set of rows includes odd-numbered rows.

* * * * *

We claim:

1. A memory array, comprising:

at least a first column of memory cells and a second column of memory cells, wherein the memory cells of the first column and the second column have a common logic and are associated with at least a first memory port and a second memory port;

first column bitlines in communication with the memory cells of the first column, the first column bitlines including bitlines in communication with the first memory port and the second memory port, wherein the bitlines associated with the first memory port include a bitline exchange associated with a first selected row of memory cells and the bitlines associated with the second memory port include a bitline exchange associated with a second selected row of memory cells, wherein the first selected row and the second selected row are different; and

second column bitlines in communication with the memory cells of the second column, the second column bitlines including bitlines in communication with the first memory port and the second memory port, wherein the bitlines associated with the first memory port include a bitline exchange associated with the first selected row of memory cells and the bitlines associated with the second memory port include a bitline exchange associated with the second selected row of memory cells.

2. The memory array of claim 1, further comprising a conductor situated between the first column of memory cells and the second column of memory cells and configured to be charged to a predetermined voltage.

3. The memory array of claim 1, wherein the conductor is configured to supply electrical power to the memory cells of at least one of the first column and the second column of memory cells.

4. The memory array of claim 1, wherein the memory cells of the first column and the second column have a common design.

5. The memory array of claim 1, wherein the memory cells are associated with a third memory port, and bitlines associated with the third memory port include bitline exchanges at one of the first selected row or the second selected row.

6. A memory, comprising:

an array of multi-port memory cells, the array associated with a plurality of columns of memory cells;

a plurality of bitlines in communication with the columns of memory cells, wherein the plurality of bitlines for each column of memory cells includes bitlines associated with the memory ports of the multi-port memory cells, wherein the bitlines associated with at least a first memory port include a bitline exchange associated with a first selected row of memory cells and the bitlines associated with at least a second memory port include a bitline exchange associated with a second selected row of memory cells, wherein the first selected row and the second selected row are different.

7. The memory of claim 6, further comprising a set of intercolumn conductors configured to be charged to at least one fixed voltage.

8. The memory of claim 7, wherein the set of intercolumn conductors includes conductors associated with a first voltage and a second voltage.

9. The memory of claim 7, wherein the bitlines and bitline exchanges associated with a selected memory port are defined in two conductor layers.

this Office action. Claims 12-15 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

7. Authorization for this examiner's amendment was given in a telephone interview with Mr. Mark Becker on February 15, 2005.

8. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Claims 12-15 have been canceled.

In claim 19, line 3, after the words "first memory port", the word --at -- has been inserted.

9. The following is an examiner's statement of reasons for allowance:

The closest prior art to the present invention is Wik et al. (U.S. Patent No. 6,370,078). Wik et al. disclosed a multi-port memory device having complementary bit lines are switched between a core cell and a modified core cell. Wik et al. failed to show or suggest the limitation of a plurality of bit lines for each column wherein bit lines associated with a first memory port include a bit line exchanged associated with a first selected row of memory cells, and the bit lines associated with at least a second memory port includes a bit line exchange associated with a selected row of memory cell, wherein the first selected row and the second selected row are different. The prior art also failed to show or suggest the steps of associating bit line exchanges with the bit lines of at least two memory ports, wherein the bit line exchanges for at least two